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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,397	05/16/2001	Frank Randolph Bryant	92-C-074D3 (STMI01-00024)	4170
30425	7590	04/20/2005	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			DUONG, KHANH B	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/858,397

Applicant(s)

BRYANT, FRANK RANDOLPH

Examiner

Khanh B. Duong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 March 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 17-23, 25 and 46-59 is/are pending in the application.
- 4a) Of the above claim(s) 17-23, 25, 58 and 59 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 46-57 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Response to Arguments***

In view of the Appeal Brief filed on November 7, 2003, PROSECUTION IS HEREBY REOPENED. However, new ground(s) of rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
- (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

**Response to Amendment**

This Office Action is in response to the amendment filed on **March 4, 2003**.

Accordingly, claims 54 and 55 were amended.

Claims 17-23, 25, 58 and 59 remain withdrawn from consideration as being directed to a non-elected invention.

Currently, claims 17-23, 25 and 46-59 are pending in the application, and claims 46-57 remain active.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 46, 48, 49, 52, 53 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Khan et al. (U.S. 4,192,059).**

Re claims 46, 48, 49, 52, 53 and 55 Khan et al. (“Khan”) discloses in FIG. 12 an integrated circuit device comprising: a substrate 3 (p-type); a gate structure, wherein the gate structure includes: a gate oxide layer 4 on the substrate 3; a nitride layer 5 over the gate oxide layer 4; and a polysilicon layer 15 over the nitride layer 5; a channel region under the gate structure; source/drain regions (n-type) in the substrate 3 adjacent the channel region; and sidewall spacers 34 located on each edge of the gate structure and lightly doped drain regions in the substrate below the sidewalls spacers 34.

Re further claims 49, 53 and 55, the claims recite the following process limitations: the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area; the source/drain regions are formed by implanting n-type impurities in the p-type substrate; and the source/drain regions are implanted after reoxidation. However, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, these limitations have not been given patentable weight.

**Claims 46, 48-52, 54 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by “Fabrication Technique for Fully Recessed Oxide Isolation”, IBM Technical Disclosure Bulletin, March 1, 1977, Volume No. 19, Issue No. 10, page 3947-3950.**

Re claims 46, 48, 49 and 54, the IBM publication above (“IBM”) expressly discloses in FIGs. 2A-2C an integrated circuit device comprising: a substrate (P-Si); a gate structure, wherein the gate structure includes: a gate oxide layer (“OXIDE”) on the substrate; a nitride layer (“NITRIDE”) over the gate oxide layer; and a polysilicon layer (“POLYSILICON”) over the nitride layer ; a channel region inherently under the gate structure; and source/drain regions (boron ions implanted regions) in the substrate adjacent the channel region.

Re claims 50-52, IBM expressly discloses in FIG. 2C: the gate structure has a peripheral edge and further including an uplift (bird’s beak) in portions of the nitride layer proximate the peripheral edge of the gate structure; the substrate has a surface and further including an indentation in the surface of the substrate located proximate to the peripheral edge of the gate structure; the gate structure includes sidewall spacers (NITRIDE) located on each edge of the gate structure and lightly doped drain regions (boron ions implanted regions) in the substrate below the sidewalls spacers.

Re further claims 49, 50, 51, 54 and 55, the claims recite the following process limitations: the nitride layer is formed by nitrogen implantation to form an implanted area and by annealing of the implanted area; the uplift caused by reoxidation of the gate structure, wherein asperities are absent from the polysilicon layer; the indentation resulting from reoxidation of the gate structure; and the source/drain regions are implanted prior to or after reoxidation. However,

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the method of forming a device is not germane to the issue of patentability of the device itself.

Therefore, these limitations have not been given patentable weight.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 47, 56 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan.**

Re claims 47, 56 and 57, Khan fails to show specific dimensional parameters of the nitride layer, gate oxide layer and channel region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Khan by selecting such dimensional parameters within the ranges as required by the claims, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

***Nonstatutory Type Double Patenting***

The **nonstatutory** double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 46-55 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 5,710,453 ("the Patent"). Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application merely broadens the claims of the Patent. For example, instead of "a gate oxide layer on the substrate, the gate oxide layer having a region thicker than a surrounding portion of the oxide layer", the present application claims "a gate oxide layer on the substrate".

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

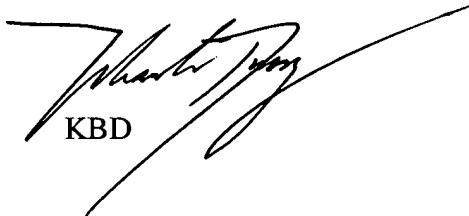
The following references disclose relevant information regarding the instant invention: JP 62079625 A, Ghezzi et al. (U.S. 4,583,281), Nguyen et al. (U.S. 4,897,364), Godejahn, Jr. (U.S. 4,506,437) and Euen et al. (U.S. 4,869,781).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (703) 305-1784. The examiner can normally be reached on Monday - Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



KBD



AMIR ZARABIAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800